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(54) Multiple port register file with interleaved write ports

(57) A high speed register file is provided for use with Very Long Word Instruction (VLIW) and N-way superscaler processors. The high speed register file includes a selected number of copies of a general purpose register (GPR) building block. The GPR building block

includes at least two interleaved sub-banks of registers. Each of the sub-banks includes a number N of write ports and a number M of read ports. The sub-banks are interleaved by write ports and have non-interleaved read ports.

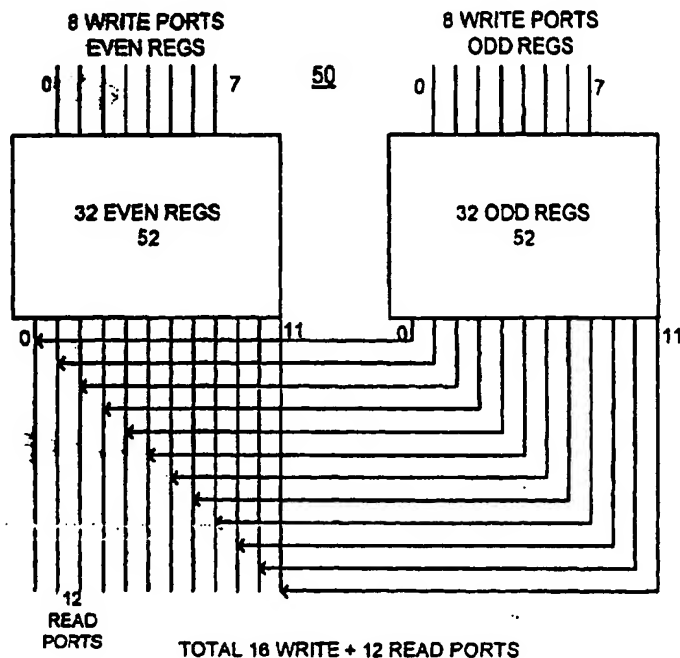


FIG.1

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Application Number
EP 96 48 0056

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| | | | TECHNICAL FIELDS SEARCHED (Int.CI.8) |
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| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 30 November 2000 | Examiner Daskalakis, T |
| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p> | | | |

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